EE 110 Practice Problems for Exam 2, Fall 2008

1. Circle T (true) or F (false) for each of these Boolean equations.

   (a). T F An 8-to-1 multiplexer requires 2 select lines.
   (b). T F A half adder has a carry input.
   (c). T F Even parity means the data has an even number of bits that are 1.
   (d). T F If a decoder has 16 outputs, it requires 3 inputs to choose all possible outputs.
   (e). T F Latches are edge-triggered memory devices.

2. Signed Arithmetic:

   2(a). Find $35_{10} - 72_{10}$ using two’s complement format with 8-bit numbers. Then convert your result back to decimal.

   2(b). Find $65_{10} - 25_{10}$ using one’s complement format with 8-bit numbers. Then convert your result back to decimal.

   2(c). Add $65_{10} + 72_{10}$ using 8-bit sign-magnitude format for the numbers. Convert your result to decimal. Is your answer correct? Why or why not?
3. Combinational Logic:

Design a circuit that counts the number of 1’s present in 3 inputs $A$, $B$ and $C$. Its output is a two-bit number $X_1X_0$, representing that count in binary. Assume active-HIGH logic.

3(a). Write the truth table for this circuit.

3(b). Find the minimized logic equations for outputs $X_1$ and $X_0$; use a K-map if needed.

3(c). Draw the corresponding logic diagram for this circuit. Label all inputs and outputs.
4. Combinational Logic: Multiplexers and Encoders

4(a). Draw a block diagram of a 4-to-1 multiplexer. Do not use a gate-level diagram. Label all inputs and outputs.

4(b). Draw a block diagram of a 4-to-2 encoder. Label all inputs and outputs. How is the 4-to-2 encoder different from a 4-to-1 multiplexer?

4(c). Write the truth table for a 4-to-2 priority encoder. Write a simplified truth table for a 4-to-1 multiplexer (hint: your multiplexer truth table should have 2 inputs).
5. Combinational Logic: Binary Adders
You wish to add two 4-bit numbers. You have half adders and full adders available to use as components.

5(a). Draw a block diagram of your 4-bit adder, using half and full adders. Do not draw a gate-level diagram. Show and label all inputs and outputs.

5(b). Assume that a half adder has a maximum propagation delay of $\Delta$, and a full adder has a maximum propagation delay of $2\Delta$. What is the maximum propagation delay for your 4-bit adder, from LSB input to MSB output?

6. Sequential Logic: Latches and Flip-flops
6(a). Draw a block diagram (not a gate-level diagram) of a D latch and a D flip-flop. Show and label all inputs and outputs.
6(b). Write the truth tables for both a D latch and a D flip-flop.

6(c). On the following graph, inputs CLK and $D$ are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the EN or C input of the D latch. Write the output of the D latch as $Q_{DL}$ on the graph. Then write the output of the D flip-flop as $Q_{DF F}$ on the graph. Ignore setup and hold time requirements (assume $T_{SU} = T_{H} = 0$). Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?
7. Sequential Logic: Counters

7(a). Design a 3-bit binary synchronous down-counter using J-K flip-flops. First, draw the state bubble diagram, showing the 3-bit flip-flop outputs as the state.

7(b). Draw the circuit diagram, using flip-flops as blocks (don’t draw the individual gates in each flip-flop). Show and label all inputs and outputs. Assume the J-K flip-flops are rising-edge-triggered.
For an output cycle of 10 clock pulses, draw the 3 outputs $Q_0$, $Q_1$ and $Q_2$ of the ripple counter on the grid below. State which output is the MSB and which is the LSB. Assume that you start in the all-zeros state (000) as shown below. Assume the J-K flip-flops are rising-edge-triggered.